REMARKS

Reconsideration and allowance of the above-identified application, as currently amended, is respectfully requested. The present amendment follows, also, the personal interview held with Examiner H. Jey Tsai on November 16, 2005. The Examiner is thanked for his courteousness in that regard.

Several amendments are being made in the Substitute Specification that are, generally, of an obvious formal nature. These revisions are being made for purposes of effecting further clarification and improving the readability thereof. It is submitted, these revisions do not raise the issue of new matter. For example, in the paragraph bridging pages 35 and 36 of the Substitute Specification, a parenthetical expression containing alternative descriptive terms for the expression "fall-in amount" was interlineated so as to clarify the intent of that expression. The interlineated expression, it is noted, is consistent with the showings, for example, in Fig. 5 of the drawings in which the "fall-in amount B" of the embedded oxide film, clearly, is shown as a depth or recess amount B. This is also consistent with the related discussion thereof on pages 35-36, etc., of the Substitute Specification. Regarding the paragraph bridging pages 37-38 of the Substitute Specification, the revision implemented therein is also strictly of an obvious formal nature, namely, to simply relate the expression "impurity peak concentration position" to an impurity profile, as should be clearly understood. This is consistent with the context of the related discussion therein. Also, in the paragraph bridging pages 55 and 56 of the Substitute Specification, the revisions implemented therein editorially clarify the intent of the related phraseology, which should be apparent from a reading thereof. These clarifications were effected noting that the discussed oxynitride film therein is

now featured in independent claims 49 and 55. In fact newly presented dependent claims 50 and 56 specifically set forth a scheme in which, also, the oxynitride film is provided in a manner consistent with the referred to "first method" in the paragraph bridging pages 55 and 56 of the Substitute Specification.

The above set forth revisions to the Substitute Specification were discussed in length in the interview held with the Examiner. It is submitted, the current revisions to the Specification are strictly of a minor formal nature such as to effect further clarification and thereby improve the readability thereof. That is, these changes do not involve the presenting of new matter, either by addition and/or deletion.

By the above-made amendments, claims 49-60 are being newly presented as a substitute for rejected claims 1-11, 45 and 46. The new claims are directed to similar subject matter covered by the previously rejected claims, as explained to the Examiner at the interview. The newly presented claims further clarify the featured aspects intended to be covered including in a manner to highlight various aspects defining over the art documents as cited in the outstanding art rejections as well as over several other uncovered U.S. patent documents, all of which were discussed in the interview held with the Examiner on November 16, 2005. The substance of the discussion regarding the uncovered patent documents will also be covered in these remarks.

Newly presented claims 49+ and 55+ set forth a semiconductor device in which a key featured aspect thereof pertains to the recess amount of the insulating film embedded in the trench of the element isolating region (e.g. STI). In this regard, both of the independent claims 49 and 55 particularly set forth a semiconductor device in which not only is there a recessed upper plane surface associated with the embedded insulating film in the trench but, also, that the embedded insulating film

with the recessed upper plane surface must surround the source and drain diffusion regions. The invention according to independent claim 49, for example, calls for a semiconductor device comprising a semiconductor substrate; an element isolating region having a trench formed in the semiconductor substrate and an insulating film which is embedded into the trench; and an active region formed in the semiconductor substrate and including a well region in which a gate insulating film is formed thereon and a gate electrode is formed on the gate insulating film, the well region having ion implanted source and drain diffusion regions.... An example of this is shown with regard to the embodiment(s) according to Figs. 1A – 1H as well as the discussion with regard to Figs. 2-16 of the drawings, in which 119 is an example of an element isolation region (STI region) which surrounds an active region 118 (see in particular Figs. 9-10 of the drawings). Also according to new independent claim 49, consistent with the example showings in the drawings, the "embedded insulating film" in the trench has a bottom surface plane that extends deeper into the substrate than that of the diffusion regions and, also, surrounds the active region, as can be seen with regard to the example Fig. 9 illustration directed thereto. Moreover, the semiconductor device is structured so that:

> "...the embedded insulating film has a recessed upper plane surface surrounding at least said source and drain diffusion regions to prevent crystalline defects caused by said element isolation region at vicinity of said diffusion regions, the recessed upper plane surface defining a depth, extended from a plane surface of said semiconductor substrate, substantially the same as or greater than that of the depth of the peak concentration of the impurity profile of each of said source and drain diffusion regions, and
> "...an oxynitride film is formed along side and bottom surface planes of the embedded insulating film in said trench and interfacing with said silicon substrate."

From the above recitation, a key aspect of the invention is the desirability of forming a recessed upper plane surface of the embedded insulating film (in the trench associated with an element isolating region (STI)) which surrounds at least the source and drain diffusion regions of an active region. In the example illustrations in Figs. 9 and 10 of the drawings, STI 119 not only surrounds the field effect transistor but, moreover, the portion thereof which surrounds the respective source and drain regions has a recessed upper plane surface. The recessing of the embedding insulating film around the entire outer periphery of the source region as well as of the drain region is further defined, according to independent claim 49, as noted above, as a recessed upper plane surface defining a depth, extended from a plane surface of the semiconductor substrate, substantially the same as or greater than that of the depth of the peak concentration of the impurity profile of each of said source and drain diffusion regions.

By implementing in the embedded insulating film such a recessed upper plane surface as that according to claim 49, crystalline defects caused by the element isolation region at vicinity of the diffusion regions are prevented. That is, the inventors have found that the recessing of the embedded insulating film over the entire outer periphery of the source region and of the drain region is necessary for relieving stress that would otherwise be caused by the presence of the insulating film near the source and drain regions, especially when high doping concentration is involved in those regions. Accordingly, the depth of the recessed upper plane surface, extended from the substrate surface, according to the invention, takes into account the depth to which the source and drain regions extend. Such depth, as noted above, should be at least as great as the depth of the peak concentration of such impurity profiles associated with the active region. Discussion regarding this is

found on page 37, line 17, et seq. of the Substitute Specification in conjunction with Fig. 5 of the drawings. For example, the impurity implanting depth may be based on the depth taken from a location on the substrate surface midway the distance between an edge of the gate electrode and the near edge STI trench (see dependent claims 54 and 60 and the related discussion in the first full paragraph on page 38 of the Substitute Specification).

New independent claim 55 calls for a semiconductor device including plural active regions and an element isolating region for mutually isolating the active regions from each other. In this regard, the device according to claim 55 sets forth a trench formed in the element isolating region into which an insulating film is embedded, similarly as that set forth according to new independent claim 49. The invention according to claim 55 covers a scheme such as that covered by previously pending independent claim 11. The corresponding dependent claims of claim 55 are similar to the corresponding dependent claims of new independent claim 49.

Another featured aspect according to new independent claims 49 and 55, recited above, concerns the formation of a oxynitride film along the bottom and sidewall surface planes of the embedded insulating film in the trench and interfacing with the silicon substrate. According to new dependent claims 50 and 56, further, this concerns the formation of oxinitride film along the bottom and sidewall surface planes at the interface between the silicon substrate and the thermal oxide film (e.g., thermal oxide film 102). This added featured aspect effects a further lowering of STI stress and is discussed in the paragraph bridging pages 55 and 56 of the Substitute Specification. The newly added dependent claims 51 – 53 and, likewise, claims 57-59 further characterize the depth of the recessed upper plane surface of the embedded insulating film. Additional discussion as it relates to STI compression

stress is covered, for example, beginning on page 32 of the Substitute Specification (see also Figs. 2-6). It is submitted, the invention according to new claims 49+ and 55+, is defining over the previously cited art documents, as applied in the outstanding art rejections and, moreover, is also defining over the newly uncovered Yamauchi, et al. (U.S. Patent No. 6,642,124 B1) and Hirai, et al. (U.S. 6,395, 598 B1) patents, which were discussed in detail also in the interview with the Examiner. The uncovered WIPO published patent application (WO 02/063690 A1) was also discussed with the Examiner.

As to the previously standing art rejections, covering claims 1-11, 45 and 46, they have been rendered moot with the canceling of these claims. The canceling of the claims should not be construed as acquiescence with regard to the merits of those rejections.

The previously withdrawn claims were also cancelled but, however, without waving Applicants' right to subsequently file a divisional application directed thereto.

The discussion to follow will show the various patentable featured aspects according to new claims 49+ and 55+ over that taught by Liaw (U.S. Patent 5,972,759), Liaw (U.S. Patent 5,930,633), Huang (U.S. Patent 6,406,987) and Nishioka (US 2002/0008019 A1), applied in the previous art rejections, and, also, over the newly uncovered patent documents, irrespective of whether the teachings thereof are applied individually or in any combination with these listings.

Hirai, et al. (US 6,395,598 B1)

In Hirai, et al. although an STI with a recessed upper surface is disclosed, the recess is not intentionally produced as a desirable structural feature but, rather, is unintentionally formed as result of the over etching produced in the formation of the sidewall insulators of the insulated gate electrode. (Column 1, lines 50-53 and 59-62

in Hirai, et al.) It is an aim of Hirai, et al. to overcome the problem of overetching which leads to the recessed STI.

Hirai, et al.'s disclosure is particularly concerned with reducing leakage currents associated with undesired recessing of the STI. Such leakage current occurs due to exposure (in the trench) of the pn junction (in the active region) which comes in contact with a conductor such as metal plug 13 in Fig. 1d. (Column 2, lines 24 – 28 in Hirai, et al.) Hirai, et al. solves this problem, for example, by effecting a scheme such as in connection with Figs. 4 and 8 thereof, in which the former uses a sidewall spacer 45b to cover the side of the stepped portion (See Fig. 4a) while the latter uses an elongated insulating sidewall spacer which is made of silicon nitride to effect electrical isolation of the pn junction between the source/drain region and the substrate (see the sidewall in 99b and the pn junction 98 in Fig. 8). In other words, Hirai, et al. is concerned with overcoming the adverse effects of the formed recessed STI, clearly unlike that according to the present invention. Hirai, et al., it is submitted, is not concerned with the STI stress concerns which applicants addressed in connection with achieving the present invention and, also, it is observed, the recessed STI in Hirai, et al. is unintentionally formed. As mentioned above, Hirai, et al. is concerned with overcoming the adverse effects such as of leakage currents and would rather avoid overetching of the embedded insulating film STI, if possible.

Yamauchi (U.S. 6,642,124 B1)

Yamauchi also features an STI in his semiconductor device. The STI in Yamauchi does surround the source/drain and, also, includes an oxynitride film which reduces compression stress. However, a main aim of Yamauchi is to minimize divot formation and occurrence of a kink and thereby reduce junction leak

current. (Column 1, line 32, to column 2, line 34, and Figs. 7-9 in Yamauchi.) Although Yamauchi is concerned with compression stress such as during the time of annealing, and does employ an oxynitride film, there is no specific discussion therein or even a hint made by Yamauchi that would have made it desirable to intentionally form a recessed embedded insulating film in the trench which surrounds the source and drain regions and in which the depth of the upper plane surface of the recessed insulating film is as that called for according to new independent claims 49 and 55 and further according to the corresponding dependent claims thereof.

Although Yamauchi is somewhat concerned with compression stress, he does not employ a recessed STI to remove crystal defects in the vicinity of the source/drain region. The formed divot in Yamauchi (e.g. 81 in Fig. 8) is unintentional, which is clearly in contradistinction with the intent of the new claims, i.e., in which the recessed upper plane surface of the embedded insulating film which completely surrounds at least the source and drain regions of a transistor element is formed by intentional design.

As noted above, an objective of Yamauchi's scheme is to effect junction leak current reduction and improve the reliability of the gate oxide insulator through minimizing divot formation and the occurrence of a kink in the transistor characteristics curve. (Column 2, lines 36-42, in Yamauchi.) In this regard, Yamauchi provides an oxide film containing nitrogen which acts as a liner oxide film along the wall of the trench to lessen the degree of distortion in the structure within the oxide film and the lowering of the compression stress on the wall of the trench. (Column 1, lines 44-55, in Yamauchi.) However, Yamauchi, like Hirai, et al., neither disclosed nor even hinted at intentionally forming the embedded insulating film with a recessed upper plane surface for the specific reasons noted and in which the

amount of the depth of the recessed surface is predetermined in accordance with claims 49 and 54 and, more specifically, in connection with other ones of the dependent claims such as new claims 55 and 60. This discussion regarding Hirai, et al. and Yamauchi was also addressed in the interview with the Examiner.

Liaw (U.S. 5,972,759 and U.S. 5,930,633)

Both of the Liaw disclosures fail to disclose or even hint at intentionally forming a recessed upper plane surface of an embedding insulating film in an STI in the manner is that now called for according to claims 49+ and 55+. In both disclosures, it is submitted, the dip in the trench does not completely surround the source/drain region, rather, the dip occurs only at small part of the surrounding outer periphery of the, for example, drain region. Moreover, Liaw ('759 and '633) is concerned with avoiding undesired short circuits between that of a higher level conductive layer with that of a lower level conductive layer caused by misalignments during the manufacture of the device.

In Liaw ('759) it is an objective to provide a manufacturing scheme for forming a butting contact that prevents an overlying conductive layer from shorting to the substrate because of a misaligned lower level polycrystaline silicon conductive line (e.g., 30B) or because of a butt contact to active region photo mis-alignment. (Column 1, lines 45 – 57, in Liaw ('759).) Another objective of Liaw ('759) is to achieve a butting contact that widens the design rules pertaining thereto. (Column 1, lines 63-65, in Liaw ('759).) In order to avoid defects because of such misalignments, Liaw ('759) has schemed fabricating a butt contact (e.g., 64) which contains protective spacers (e.g., 50A) to protect against shortings due to misalignments. (Column 1, line 66, to column 2, line 2; column 2, lines 47-48, and 65-67; column 3, lines 6-8, lines 9-22 and lines 49-52; column 4, lines 14-38; column

6, lines 24-45, etc., in Liaw ('759).) Such discussion is also applicable with regard to Liaw ('633). In other words, Liaw ('759 and '633) is not concerned with the problems to which the present inventors addressed which has led them to intentionally form the STI with a recessed upper plane surface of the embedded insulating film which surrounds the outer periphery of both the source and drain regions and, moreover, in which the depth of the recessed surface is determined by the impurity profile of the source/drain regions. Moreover, Liaw ('759 and '633), it is submitted, does not teach using a oxynitride film nor or is concerned with compression stresses associated with the STI which has led the present inventors to achieve a schemed recessed embedded insulating film as that now called for in each of 49+ and 55+.

Huang (U.S. 6,406,987 B1)

Huang also failed to disclose or suggest a recessed height (depth) of the embedded insulating film in the trench to the degree of specificity set forth in claims 49+ and 55+. Also, Huang does not disclose or even hint at avoiding compression stress nor, for that matter, does Huang even hint that any recessing occurrence of the STI thereof is intentionally made. It is an aim of Huang to likewise prevent contact short circuits between the source/drain and the substrate and, also, eliminate erosion of the gate oxide to prevent gate/drain shorts. Huang employs, for example, "visors" (e.g., visor 20" in Fig. 10) to fill undesired dips such as to prevent electrically shorts. (Column 5, line 45, et seq. and column 6, lines 30-35 and Fig.10 and lines 49, et seq. and Fig. 12.)

Nishioka, et al. (U.S. 2002/0008019 A1)

It is observed that Nishioka, et al.'s scheme does not call for a recessed embedding insulating film in the manner as that currently called for in each of the independent claims 49 and 55 and, more particularly, with regard to the

corresponding dependent claims thereof. In fact, Nishioka, et al. is not concerned with problems to which the present inventors address.

WIPO International Patent Publication (WO 02/063690 A1)

This publication which was also discussed with the Examiner during the held interview shows an oxide-nitride film or silicon nitride film formed on the surface of the thermal oxide film, as noted in the English abstract thereof. However, there is neither any showing or suggestion therein of a recessed STI in the manner called for in according to the new claims 49+ and 55+.

It is submitted, none of the references cited in the last Office Action or even the three uncovered patent documents, each applied separately or in any combination, taught the schemed invention as now set forth according to new claims 49 – 54 and 55 – 60. Such was also emphasized during the interview held with the Examiner.

In consideration of the above discussion and the discussion held with the Examiner, examination as well as favorable action of the newly presented claims 49-60 as well as an early formal notification of allowance of the above-identified application is respectfully requested.

Statement of Substance of Interview

The Examiner's summation in the Interview Summary Form PTOL-413, dated November 16, 2005, is correct. In supplement thereto, it should be noted that all of above-named references applied in the art rejections of the outstanding Office Action along with the three (3) newly uncovered art documents were discussed with the Examiner, the details of which are further highlighted in these responsive remarks.

If the Examiner deems that questions and/or issues still remain which would prevent the present application from being allowed at the present time, he is urgently invited to telephone the undersigned representative, at the number indicated below, so that either a telephone or personal interview may be arranged at the Examiner's convenience in order to discuss the same and hopefully resolve any remaining questions/issues present.

Applicants request any shortage of fees due in connection with the filing of this paper, including extension of time fees, be charged to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (case 500.42877X00), and credit any excess payment of fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Larry N. Anagnos
Reg. No. 32,392

LNA/gjb
1300 N. Seventeenth Street
Suite 1800
Arlington, Virginia 22209
Tel: 703-312-6600
Fax: 703-312-6666